High density Integrated Optoelectronic Circuits for High Speed Photonic Microsystems

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Abstract. The study of high density integrated optoelectronic circuits involves the development of hybrid integration technologies and the generation of models for the optoelectronic devices. To meet these goals, in the beginning a methodology for the heterogeneous integration of epitaxial GaAs wafers with fully processed standard bipolar complementary metal-oxide-semiconductor Si wafers is presented. The complete low-temperature wafer bonding process flow, based on SOG/SIO_2, including procedures for the Si wafer planarization and GaAs substrate removal, has been developed and evaluated. The implementation of an in-plane optical link, consisting of an edge-emitting laser diode, a waveguide and a photodiode, is demonstrated. Further investigation on heterogeneous integration is achieved by presenting a second methodology. The integration of complete optoelectronic dies, consisting of optical sources and detectors connected by waveguides for the employment of a photonic layer above CMOS integrated circuits has been proposed. Photonic dies are integrated to CMOS circuits through a novel metallic bonding technique that utilizes a thin multilayer structure of the Au-20Sn eutectic alloy along with a starting layer of a rare earth element (Gd). Its main advantage is the accomplishment of mechanical bonding and electrical connectivity of the heterogeneous devices in a single step. The study of photonic microsystems demands also the modeling of specific OE devices. Under this scope, an efficient model scheme that combines the non-linear behavior of the input parasitics with the intrinsic fundamental device rate equations of the Vertical Cavity Surface Emitting Lasers (VCSELs) is proposed. A systematic methodology for the model parameter extraction from dc and ac, electrical and optical measurements, is also presented and simulation results are compared with the experimental measurements. Extraction and simulation procedures are implemented in commercial integrated circuit design tools and they are proved to be very fast while they preserve adequate accuracy.

Keywords: heterogeneous integration, SOG/SiO_2, photonic link, metallic bonding, Au-80Sn, VCSELs, circuit model, parameter extraction, rate equations.

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1 Hybrid Integration-Technologies

High-density optical interconnections require the integration of III–V optoelectronic (OE) devices along with Si integrated circuits (ICs). Currently, hybrid integration, based on flip-chip bonding, is the most mature technology for the combination of III–V optoelectronics with Si ICs [1]-[2]. The main drawback of the hybrid approach is the demanding fabrication sequence which results in increased manufacturing cost. A different approach for the integration of Si ICs with III–V OE devices is the fabrication of the OE devices in layers grown by heteroepitaxy on the Si wafer. However, the heteroepitaxial approach suffers from poor III–V material quality. Furthermore, process incompatibilities and cross contamination problems, between the complementary metaloxide-semiconductor (CMOS) and III–V technologies, cannot be easily eliminated.

In order to overcome the limitations of the hybrid and heteroepitaxial integration, we have developed a process having the wafer-scale characteristics of heteroepitaxial integration and at the same time being compatible with commercial bipolar CMOS (BiCMOS) technology. Our first approach is a low-temperature (LT) process, employing SiO_2 and spin-on glass (SOG) layers for the planarization and bonding of epitaxial GaAs wafers onto fully processed BiCMOS wafers. The second approach for hybrid integration that we propose is based on the use of a metallic alloy. This metallic bonding methodology is introduced for bonding OE dies above CMOS circuitry and it is based on the use of a proposed multilayer structure of Au-20Sn eutectic alloy over a thin film of Gd, as bonding agent.

1.1. Bonding with SOG/SiO_2

The basic process flow for the wafer-scale integration scheme starts with the fabrication of the ICs on a 4 in. Si wafer using a commercially available BiCMOS technology and the OE device layers are grown on a 3 in. GaAs wafer. The OE device layers are grown with the inverse sequence of the regular device structure, after the epitaxy of a thin AlAs etch-stop layer. Then, the fully processed Si wafer is covered by successive SiO_2 layers, deposited at low temperature (LT) using plasma enhanced chemical vapour deposition (PECVD), and the surface is planarized by chemical mechanical polishing (CMP). Next, the planarized and polished SiO_2 top layer is covered by SOG, to eliminate any remaining surface imperfection and to act as a bonding agent. Subsequently, a proper baking procedure is followed to remove the volatile elements from the SOG before the wafer bonding. The Si wafer is then bonded at room temperature face to face with the epitaxial GaAs wafer. The two wafers are centered and their major flats are mechanically aligned. The bonding is further strengthened by an annealing step performed at 200°C (the temperature must be kept below 250°C to avoid debonding due to the difference in the thermal coefficients of expansion (TCE) of GaAs and Si). The backside of the entire GaAs substrate is then removed by an appropriate thinning process so that only the epitaxial III–V structure remains bonded onto the top surface of the BiCMOS wafer. After this stage of the process flow the

temperature can rise up to 400 °C because the constraint of the different thermal coefficients of expansion becomes more tolerant due to the preceding thinning of the GaAs wafer, which can now sustain larger deformations. The remaining III–V film is thereafter processed to form OE devices using conventional III–V processing technology. The mask alignment of the OE devices to be fabricated on the bonded GaAs film can be performed either by infrared backside alignment or by alignment marks placed on the uncovered annulus of the 4 in. silicon wafer. The final steps of the process are: (a) the opening of via holes through the III–V film and the insulating intermediate layers and (b) the fabrication of electrical interconnections between the Si ICs and the OE devices using either wire bonding or on-wafer metalizations.

In order to evaluate the critical steps of the process flow, we have undertaken a series of experiments focusing on different aspects of the process. Both unprocessed and fully processed BiCMOS 4 in. Si wafers were bonded with 3 in. epitaxial GaAs wafers. The processed Si wafers were fabricated with the commercially available 0.8 mm BiCMOS technology of Austria Mikro Systems AG (AMS™). The epitaxial GaAs wafers consisted of various GaAs/AlGaAs heterostructures [3] grown by molecular beam epitaxy (MBE). The investigation of the LT SiO_2 /SOG based wafer bonding process has been initiated with the examination of the surface morphology of the commercial fully processed BiCMOS wafers. Atomic force microscopy and profilometry showed that the two-level metal interconnection stripes presented unevenness of 0.6–1.3 mm. Furthermore, irregular edges of 2 mm height existed in the IC testing pads opened within the capping nitride layer. This surface unevenness was reduced to about 90 nm by the planarization procedure. For that purpose, multiple low-temperature oxide layers, with 2mm total thickness, were deposited by PECVD and then polished using fumed silica as polishing media. Further planarization was accomplished by deposition of a SOG layer so as to achieve the bondability condition (microroughness under 1 nm). The average interface energy of the bonded surfaces was measured using the crack opening method by inserting a blade between the bonded wafers. The interface energy, before annealing, was 0.46 J/m^2 and reached the value of 1.4 J/m^2 after annealing at 200°C. The backside thinning of the bonded GaAs substrates has been investigated using two different methods. In one approach, CMP was used to thin the 400-mm-thick GaAs substrates to approximately 30 mm while in the second approach the GaAs substrates were thinned to an average thickness of 80 mm, using a fast wet etching process (using H_3PO_4:H_2O_2:H_2O). Laser diodes (LDs) have been fabricated on films bonded onto fully processed BiCMOS wafers and compared to similar devices processed on GaAs substrates.

In order to demonstrate the feasibility of the entire process, a complete in-plane OE link [4] was designed and fabricated. The link consists of a BiCMOS laser diode driver (LDD), an edge-emitting LD, a planar waveguide (WG), a photodiode (PD) and a BiCMOS transimpendance amplifier (TIA) [5]. The output of the laser driver was designed to be at a distance of 500 mm from the input of the TIA. In the space of 500 mm are placed the LD, the WG and the PD so as to form a complete OE link. The microphotograph of the integrated OE link is shown in Fig. 1.

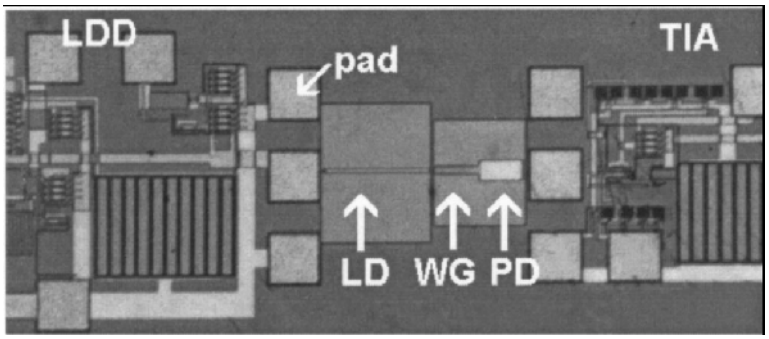


Fig. 1. Nomarski optical microscopy image showing the fabricated LD-WG-PD GaAs optical link.

The entire OE link was also successfully tested, unpackaged, for its functionality under low duty-cycle pulsed signal operation (0.4ms pulse width and 10KHz repetition rate). High frequency characterization has not yet been attempted because the self-heating effects on the unpackaged OE link can be deleterious for the OE devices. Furthermore, the influence of the wafer bonding and the subsequent GaAs process on the Si ICs has been examined using on-wafer *S*-parameter measurements up to 8GHz. Discrete devices as well as Si ICs were characterized before and after the wafer bonding process and no apparent performance degradation was observed

1.2. Metallic Bonding

Environmental friendly processes restrict solders used in packaging to the Pb-free group. On the other hand, successful flip-chip assembly is favored by eutectic alloys. Since die attachment is realized by solder fusion, a low melting point is desirable for CMOS and OE devices thermal reliability. Various candidates, such as Sn-Ag [6-7], In-Ag [8] or Au-Sn [9-10] alloys fulfill the former requirements. The reasons for selecting 80/20 weight percent (w.t.%) Au-Sn alloy among them are its physical and thermal properties. As a hard solder it remains in elastic deformation and the thermal expansion coefficient (TEC) mismatch becomes important only when bonding large chips. Moreover, its high thermal conductivity provides adequate power dissipation. It is compatible with III-V device metallization and its advantage over other hard solders is the comparatively low melting temperature (280^{o}C), as verified by the binary phase diagram of the Au-Sn alloy [11].

In order to control accurately the alloy composition and accomplish adequate intermixing during fusion, a multilayer structure of the alloy is adopted. In addition to that, rare-earth participation in the solder is exploited by the incorporation of Gd, since rare-earth elements improve adhesion to passivating surfaces, such as SiO_2. The following step is to integrate the optical link over CMOS circuitry lying in wafers with a passivated surface. Therefore, sample bonding via metallization on bare Si as well as on SiO_2 is investigated. Consequently, an initial thin film of 50nm vacuum-evaporated Gd, which corresponds to 3.5w.t.% of the solder, can precede alternating Sn and Au

layers of appropriately selected thickness preserving the Au-20Sn eutectic alloy composition. The Sn, Au layers, also deposited by evaporation in vacuum to reduce oxidation, ranged between 250nm and 750nm in total thickness. Au has been used as a cap layer to prevent alloy surface oxidation. Either full SOI-wafer to CMOS-wafer bonding or SOI-die to CMOS-wafer bonding can be followed.

Alloy patterning capability by standard lithography processes has been verified by fabricating pads of varying thickness and diameter on 4-inch Si wafers. The ability of precise patterning over both planar and structured substrates has been examined. Since contact pads provide point-to-point electrical connectivity to optoelectronic/CMOS devices, their pitch is critical in case of alloy spreading during fusion, which could cause short circuits and therefore device malfunction. To confirm the degree of spreading, samples containing pad arrays were flipped over SiO_2 substrate, while they were annealed at 330^{o}C and pressed by 2.5MPa. An alloy spreading less than 1μm has been observed. This fact enables dense CMOS/optoelectronic device integration.

A variety of bonding experiments have been conducted in order to determine the conditions to be followed for successful bonding results. All bonding experiments took place at an annealing temperature of 330^{o}C in ambient forming gas (95%Ar-5%H_2) for 40min. The annealing temperature of 330^{o}C is within the allowed post-processing thermal range for CMOS device functionality [12-13]. On the other hand, Sn is expected to segregate to the surface of the Au-rich alloy, due to its lower surface free energy compared to that of Au. This creates a Sn-rich surface layer, which is oxidized even in a very small amount of O_2, i.e. in ambient 95%Ar-5%H_2 gas, despite the retarding influence of H_2 in oxidation. The surface oxide formation, which is a major obstacle for the bonding process, is broken up with pressure application during annealing.

The samples used in bonding experiments have a surface ranging from 0.25cm^2 to 1.5cm^2. Samples have been fabricated by direct deposition of the Gd-(Au-20Sn) alloy on substrates such as Si, SiO_2 and BCB on Si. Additional samples were fabricated by depositing the Gd-(Au-20Sn) alloy on Al or Ti/Cu layers over Si and SiO_2 substrates to examine the possibility of bonding above standard CMOS metallization schemes.

Table I summarizes the parameters for five experiments using pairs of dies with different topologies. The total alloy thickness is 800nm, consisting of 50nm Gd followed by 750nm of Sn/Au alternating layers. In the cases (c)-(c) and (d)-(d) 16 cross-section squares are formed with an area of either (100x100)μm^2 or (50x50)μm^2, respectively. In Table I, S_{total} stands for the total die area, S_{bond} refers to the contact area between flipped samples and R is the overlap ratio of S_{bond} over S_{total}. P is the pressure applied on the bonding surface (actually flipped dies accept the same force in all cases, while the pressure increases due to decrease of the contacting area) and V_{bond} stands for the total alloy volume participating in bonding. Die shear strength tests for 0.25cm^2 samples have shown a 25g/mm^2 shear stress to be sufficient for detaching the die off the host substrate, revealing edge effects prohibiting the achievement of adequate bonding strength. However, for 1.5cm^2 samples with bonding area and overlap ratio larger than 2mm^2 and 1.1% respectively, shear strength has exceeded 2.5kg, complying with MIL-STD-883G, Method 2019.7 [14].

1. DIE PAIR	1. (a)-(a)		1. (a)-(c)	1. (a)-(b)		1. (c)-(c)	1. (d)-(d)
2. S_{total} (mm^2)	2. 25	2. 150	2. 150	2. 25	2. 150	1. 150	1. 150
3. S_{bond} (mm^2)	3. 25	3. 150	3. 4	3. 1.1	3. 2	2. 0.16	2. 0.04
4. R (%)	4. 100	4. 100	4. 2.67	4. 4.4	4. 1.3	3. 0.11	3. 0.03
5. P (MPa)	5. 0.2	5. 0.03	5. 1.2	5. 4.5	5. 2.5	4. 30.6	4. 122
6. V_{bond} 7. ($10^{-3}mm^3$)	6. 50	6. 240	6. 6.4	6. 2.2	6. 3.2	5. 0.26	5. 0.06

TABLE I. Parameters of bonding experiments with the 800nm thick Gd-(Au-20Sn) alloy

Moreover, since the proposed methodology is oriented to wafer scale integration, bonding experiments of multiple dies over specific regions of an entire 4-inch wafer have also taken place (Fig. 2). In this case, coarse alignment using alignment marks on the wafer surface and accurate die dicing has been successfully accomplished. For the fine alignment of dies to wafer pads with 10μm accuracy, either a passive or an active alignment methodology should be used [15]. An alignment technique using convex and concave features on both surfaces is under development.

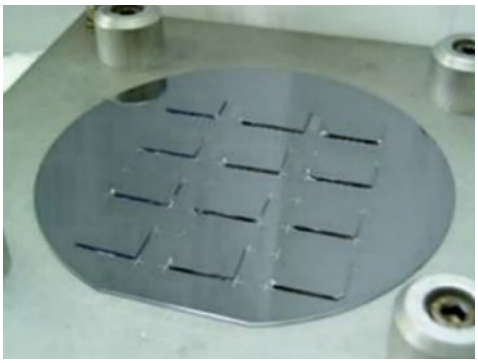


Fig. 2. Four-inch Si wafer with multiple dies bonded on specific regions

The metallic bonding technique possesses the advantage of achieving adhesion and electrical connectivity in a single step. The electrical properties of the Au-20Sn alloy are derived through a series of electrical measurements before and after it is annealed. Electrical tests are performed on mm-long alloy lines, which vary from 50μm 100μm in width. Carrier confinement across such lines ensures consistent results out of I-V testing.

Typical I-V characteristics for a 4mm long and 50μm wide line before annealing as well as for a 4mm long and 100μm wide line after annealing at 330°C are shown in Fig. 3. These I-V curves translate into a sheet resistance of 150mOhm/sq and 1.1Ohm/sq before and after the annealing respectively.

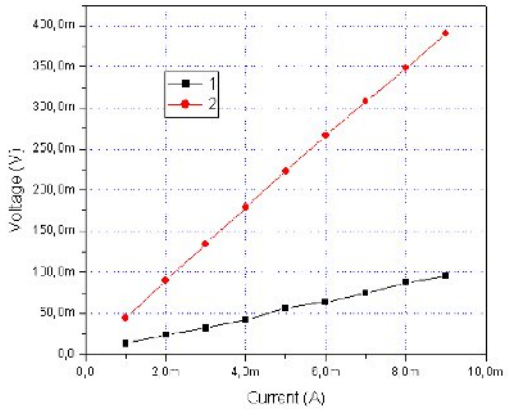


Fig. 3. I-V curves for alloy lines 4mm long and (1) 50 μm wide before annealing, (2) 100μm wide after annealing

2 OE Device Modeling

In recent years the Vertical Cavity Surface Emitting Lasers (VCSELs) have emerged and threaten to supplant the standard laser technology in a variety of applications, such as short haul high speed networks and Micro-Opto-Electro-Mechanical Systems (MOEMS). Two-dimensional VCSEL arrays are key components for achieving the highest aggregate bandwidths in tomorrow's parallel optical transceivers. Fabrication of 2D VCSEL array with 4 x 8 elements [16] as well as successful integration of 2x10 arrays of VCSELs with gigabit-per-second CMOS circuits have been reported [17].Thus, motivated by the fact that the ability to model VCSELs is critical to the design and analysis of optoelectronic microsystems, we propose a new model scheme, based on equivalent circuit optimization methodology, which will combine the non-linear behavior of the input parasitics with the intrinsic fundamental device rate equations. The complexity of the model requires a systematic methodology for the extraction of the parameters. The performed dc measurements at different temperatures as well as the ac s-parameter measurements provide a combination of electrical and optical data sufficient to define all the related parameter values. The results are validated through comparisons with simulation and measured data taken from commercially available VCSEL devices. The complete extraction procedure which has been developed proved to be very fast while it preserves adequate accuracy.

2.1. VCSEL model

The proposed circuit model for a packaged VCSEL is illustrated in Fig. 4. L_0, R_0 and C_0, model the connection to the measurement equipment and inductance L_p with capacitance C_p represent the parasitics of the package-leads as well as the wire- bonds of the package. The intrinsic VCSEL is modeled by a series resistance R_a in shunt with a non-linear capacitance C_j and the combination of a non-linear temperature-dependent current-controlled voltage-source *Einp* with a series resistance R_{int} and an ideal diode D_{vcsel}. Intrinsic voltage drop *Einp* and the intrinsic capacitance of the VCSEL are modeled according to the semi-empirical equation and to the junction diode's equation presented in [18]. The internal device temperature *T,* the carrier density and the photon density, which is equivalent to the output optical power *L*, are dynamically calculated using the respective rate equations. Moreover non-linear gain and transparency number and temperature dependent leakage current are included in the model.

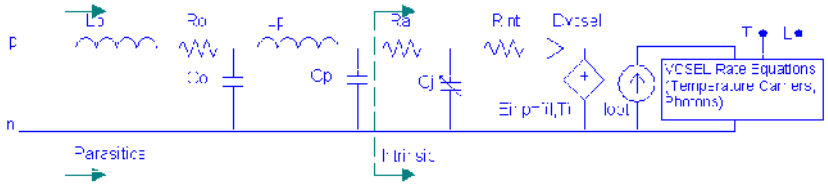


Fig.4. The proposed circuit model for the VCSEL

Since a circuit simulator is a differential equation solver, the rate equations can be solved with such a tool by mapping the dynamic quantities (i.e. the electron and photon populations) into node voltages, which are dynamically calculated. Working towards this direction, we have implemented all rate equations based on the analysis of Mena [19] in OPSIM™ of Anacad®. As an example in fig.5 is presented the equivalent circuit (with the expressions for the circuit elements) that corresponds to the following photon density equation:

$$\frac{dS}{dt} = -\frac{S}{\tau p} + \frac{\beta}{\tau n} No + \frac{Go \cdot zn\left(\gamma_o No - \gamma_1 N1 - \gamma_o Nt \cdot zn\right) S}{1 + \varepsilon S}$$

Where τp, τn, β, *No*, *Go*, γ_o, γ_1 and ε are model parameters and *zn* is an arbitrary constant used for convergence purposes.

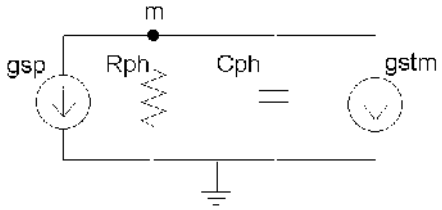


Fig.5. Equivalent circuit for the photon rate equation

$$g_{sp} = \frac{\tau p \cdot \beta \cdot k_f \cdot No}{\tau n \cdot \left(V(m) + \delta_m\right)}$$

$$g_{stm} = \tau p \cdot zn \cdot G_o \cdot \frac{\left(\gamma_o No - \gamma_1 N1 - \gamma_o N_t zn\right) \cdot \left(V(m) + \delta_m\right)}{1 + \varepsilon \dfrac{\left(V(m) + \delta_m\right)^2}{k_f}} - \delta_m$$

$$C_{ph} = 2 \cdot \tau p$$

$$R_{ph} = 1 \qquad and \qquad S = \frac{\left(V(m) + \delta_m\right)^2}{k_f}$$

2.2. Parameter extraction procedure

Due to the large number of the model parameters (16 for the input circuit and 25 for the rate equations) a three-step parameter extraction methodology is proposed to estimate them by dividing them into distinct groups. The parameter estimation is achieved by using I-L-V dc characteristics measured at four ambient temperatures and S_{11} and optical signal ac responses for various bias currents. The optimization algorithm is taken from the OPSIM™ tool, a modified Levenberg-Marquardt method, which efficiency and robustness have been proven by years of usage. In the first step the dc dependent parameters of the input circuit (such as $R_{in,}$ R_{int} and R_a) are estimated using as input to the optimization tool the dc current-light (I-L) characteristics and as targets the measured I-Vs. In the second step, using the previously calculated values, the optimization target is changed to S_{11} vector measurements and the remaining parameters of the input circuit, which influence its ac behavior (such as L_o, R_o, C_o, L_p, and C_p) are estimated. In the above procedures the rate equation that affects the results is only the thermal one, which is used to determine the internal device temperature. Thus, in the third step, the parameters of the carrier and photon rate equations as well as gain, transparency number and leakage current parameters are estimated using as optimization targets the dc I-L characteristics and the ac optical response. In Table II it is presented the flowchart of the generic algorithm used for the complete parameter extraction procedure. It is clearly illustrated the crucial dependence of each step on the results of the previously completed ones. Also Table II summarizes the grouping of the parameters depending on which extraction step procedure is applied. As it is shown in Figures 6 and 7 satisfactory agreement between measured values and simulation results for a commercially available VCSEL is achieved using the proposed model and extraction methodology. Uniqueness of the extracted parameters is not a constraint since the only limitation of the method is the convergence between measured values and simulation results.

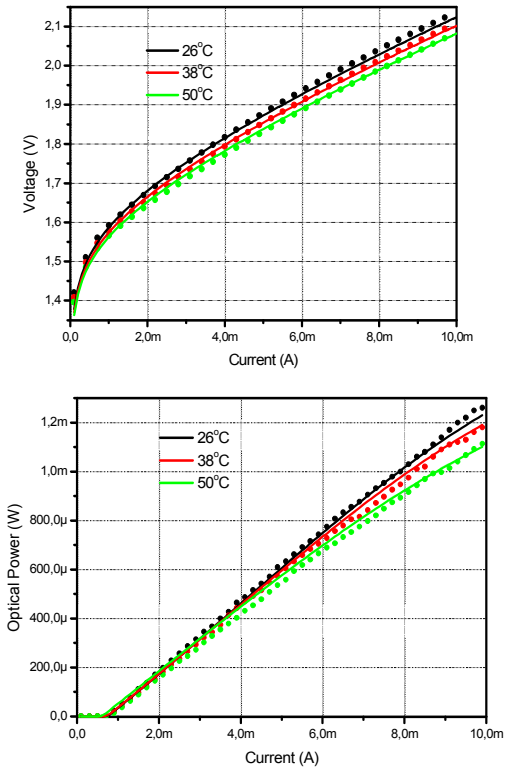


Fig.6 Measured values (dots) and simulated (continuous line) (a) I-V and (b) I-L characteristics at 26ºC, 38ºC and 50ºC.

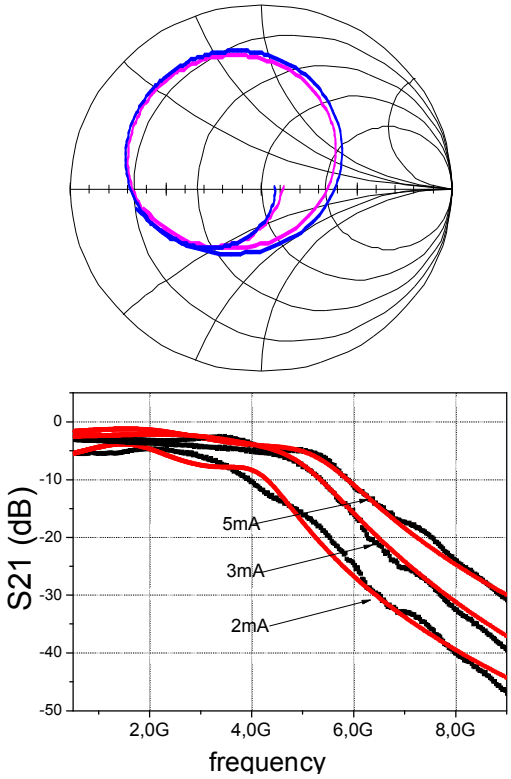


Fig.7 Measured (dots) and simulated (continuous line) S_{11} parameter at a bias of 3mA and S_{21} at 3 different biases

2.3. Driving VCSELs

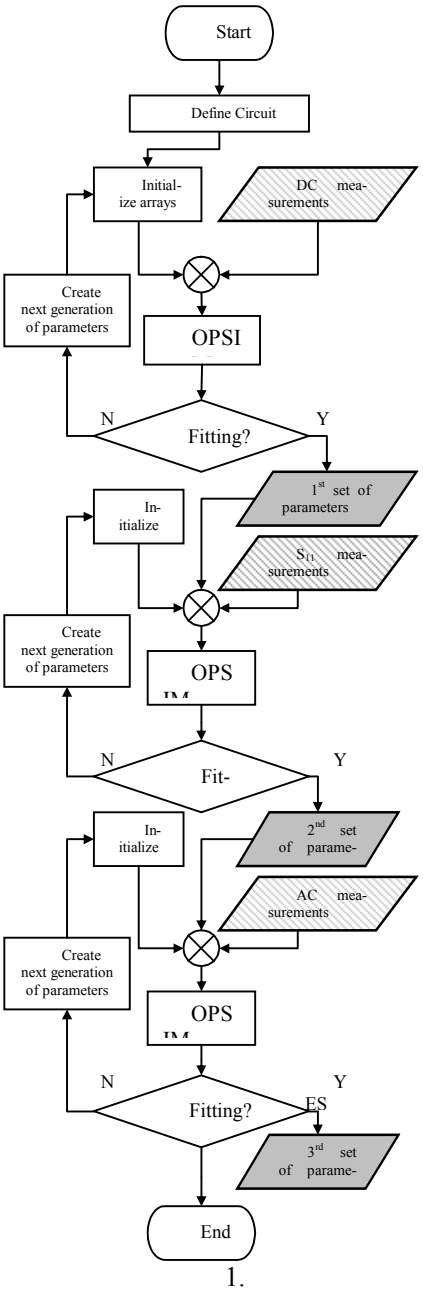
The design of a laser diode driver (LDD) is a challenging task since clear eye diagrams at high speeds require abrupt signal edges and low jitter. Traditionally, the LDDs were designed to drive Edge-Emitting Lasers (EELs) and were based on differential pair topologies acting as current-pulse sources for the laser diodes. This choice of the circuit topology is straightforward for the EELs exhibiting low series resistance very often combined with considerable series parasitic inductance. At first glance, the design task of LDDs for VCSELs seems relaxed due to the lower threshold and modulation currents required by these devices. However, high-speed VCSELs present significantly larger series resistance in combination with relatively high shunt capacitance than EELs leading to distinct requirements and consequently different design

approaches for the LDD. The particular aspects of the VCSEL drivers become crucial especially at the multi-Gb/s data rates because the packaging parasitics further aggravates the shunt capacitance effect. A comparison of the small signal and the transient response of high-speed VCSELs using ideal as well as realistic current and voltage drivers is performed. A non-linear VCSEL equivalent model is implemented and the associated parameters are extracted from dc and ac measurements of a commercially available packaged device. Simulations, using the extracted realistic VCSEL models, show that the employment of voltage drivers results in an improvement of 74% of the 3-dB cut-off frequency of the optical current signal. Moreover, an 80% reduction of the rise and fall time and a 66% reduction of the signal delay are observed.

3 Conclusions

We have proposed two different approaches for hybrid integration of OE devices on Si wafers. The reported results on the methodology using SOG/SiO_2 have clearly demonstrated the feasibility of the monolithic-like process flow for the integration of GaAs OE devices on fully processed Si ICs. Further improvement of the planarization of the BiCMOS wafer will greatly upgrade the value of the entire process. Also, a metallic bonding technique permitting dense integration of photonic structures on CMOS wafers has been proposed. A multilayer metallization structure with well-controlled alloy composition has been developed and precise as well as uniform lithographic patterns of the bonding alloy have been reproduced at a 4-inch scale. The ability to achieve bonding of various passivatiing surfaces and standard interconnect metallizations has been shown.

Investigating OE devices, a compact and efficient model for the VCSEL that models by means of equivalent circuits the fundamental device rate equations, the thermal effects, the non-linear gain and transparency number functions and the input parasitics elements has been presented. The parameter extraction is based on standard dc and ac measurements and it is achieved by a three-step procedure, which divides model parameters into distinct groups.



1.

	Symbol	Description
1st step	R_{in}	*internal resistance at temperature T_0*
	T_0	*effective reference*
	n_f	*thermal-voltage sensitivity factor*
	B	*saturation current at temperature T_0*
	C	*material related constant*
	n	*temperature exponent of the saturation current*
	R_a	*access resistance*
	R_{int}	*series resistance*
2nd step	C_{jo}	*zero bias junction capacitance*
	Φ_o	*built-in junction voltage*
	m_p	*grading coefficient*
	C_p, L_p	*parasitics of the package*
	C_0, L_0, R_0	*parasitics of the connector*
3rd step	Il_0,a_0,a_1,a_2,a_3	*Leakage parameters*
	Nt_0	*Temperature independent transparency*
	cn_0,cn_1,cn_2	*Transparency number fitting constants*
	G_0	*Temperature independent gain constant*
	$ag_0,ag_1,ag_2,$ bg_0,bg_1,bg_2	*Gain fitting constants*
	T_{therm}	*Thermal time constant*
	a	*Ratio W_m/W*
	β	*Spontaneous emission coupling coefficient*
	h_1	*Parameter modeling diffusive effects*
	ε	*Gain saturation factor of mode 0 due to mode*
	k_f	*Output-power coupling coefficient of*
	t_p	*Photon lifetime*
	t_n	*Carrier lifetime*
	n_i	*Current injection efficiency*

1.

TABLE II Flowchart of the 3-step parameter extraction procedure and model parameters

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