

CV of Constantin (Costas) Halatsis
Emeritus Professor of University of Athens, GR

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Synopsis: Constantin (Costas) Halatsis was born in Athens, Greece, in 1941. He received his B.Sc. degree in Physics in 1964 and his M.Sc. degree in Electronics in 1966, both from the University of Athens. In 1971 he received his Ph.D. degree in Computer Science from the University of Manchester, UK. From 1971 to 1981 it worked as researcher in the Centre of Computers of NCSR Demokritos, Greece, from where he retired as the Director of the Centre. In 1981 were elected Full Professor in the chair of Computers of the Department of Physics of the Aristotle University of Thessaloniki and in 1988 he was invited as Full professor in the Department of Physics University Athens. A year later he moved to the newly established Department of Informatics of the University of Athens, which in the year 2000 the Department was renamed as Department of Informatics and Telecommunications (see <http://www.di.uoa.gr>). Professor Halatsis served the Department until August 2008, and since then he is an Emeritus Professor of the Department. During 2015-17, Professor Halatsis has been with the Neapolis University Pafos of Cyprus in setting up a School of Information Sciences for offering BSc and MSc studies respectively in the fields of Applied Informatics and Information Systems. Currently, he is a free lancer consultant. For the five-years period 1988-93 he was elected Director of the Institute of Informatics and Telecommunications of the NCSR Demokritos. Also at intervals and for three years in total he worked as visiting Scientific Associate in the Data Handling Division of the European Organization for Nuclear Research CERN in Geneva, Switzerland, where he designed and built advanced Hardware processors and innovative Software. Also, during the academic year 2007-08 he has been visiting Professor in the University of Cyprus and the Open University of Cyprus. Prof. Halatsis has taught a large number of different courses at the undergraduate and postgraduate levels and it has supervised the doctoral thesis of many students, some of which are today Professors in Greek Universities. It has been financed for several European and national research programs and he has compiled and publishes in international journals and conference proceeding more than 150 technical papers after peer review and he has enjoyed international recognition. His main research area is that of Computer Architecture, both at the single processor level and that of multiprocessor systems (Von Neumann and non Von Neumann types of Architecture) for high performance computing and networking, HPCN. He has conducted research in several other areas of CS, the main of which are in the areas of Artificial Intelligence (Logic Programming, Constraints Logic Programming, CLP), Software Eng, e-government, e-learning (affective computing). His recent personal research activity is focused in fundamental open theoretical problems in Computer Science, continuing at the same time research on previous subjects. In the R&D side his recent activity is focused in the use of Virtual Reality for Cultural applications and on

issues of Electronic Governance, e-gov, eID and Data Warehouse for the Cyprus Government.. Prof. Halatsis has served at various academic positions, he has participated in a number of international and national committees and councils, and he has served as member in many international and national evaluation committees for academic positions and R&D proposals. He has studied and designed large projects of national and international Information Systems and has contributed decisively in the growth and operation of the Faculty of Science and Technology of the University of Peloponnese, GR.

Detailed CV

Personal data

Name: Constantin (Costas) Halatsis

Title: Emeritus Professor of Computer Science, University of Athens, GR

Marital status: Married, two daughters, one grandson and one granddaughter

Studies

- 1964: B.Sc. in Physics, University of Athens, GR
- 1966: M.Sc. in Electronic, University of Athens, GR
- 1971: Ph.D. in Computer Science, University of Manchester (UMIST), UK.

Professional Qualifications

- 9/2008 - Today Emeritus Professor, Dept. of Informatics and Telecommunications, Univ. of Athens, GR
- 7/2017 – Today : Free Lancer Consultant
- 9/2014 - 6/2017: Professor of Informatics, Neapolis University Pafos, Cyprus
- 9/2009 – 8/2013: Consultant to Cyprus Government, the Department of Information Systems on e-Governance issues (government gateway, electronic identification, eID and Data Warehouse-Data Mining)
- 9/2009 – 6/2012 Teaching at Open University of Cyprus
- 9/1988 – 8/2008 Full professor of CS at the University of Athens, Department of Informatics and Telecommunications, GR
- 9/2007-8/2009 Visiting Professor at the University of Cyprus and the Open University of Cyprus
- 1988 - 1993 Director of the Institute of Informatics and Telecommunications of NCSR Demokritos, Athens, GR (in parallel with the position at the University of Athens)
- 1981 - 1988 Full professor of CS at the Aristotle University of Thessaloniki, GR
- 1985 - 1987 and 1978 - 1979 Scientific Associate of Data Handling Division CERN, Geneva, CH
- 1979 - 1981 Director of the Computer Centre of NCSR Demokritos, Athens, GR
- 1971 - 1979 Research Scientist at the Computer Centre of NCSR Demokritos, Athens, GR

Academic and Administrative positions served

- **Dean** of Faculty of Sciences in the Aristotle University of Thessaloniki, GR
- **Chairman of Department** in the University of Athens and in the University of Peloponnese, GR
- **Member of Senate** of the University of Athens and of the Aristotle University of Thessaloniki, GR.
- **Director** of the Institute of Informatics and Telecommunications, NCSR Demokritos, Athens, GR.
- **Chairman** of the Department of Informatics and telecommunications, University of Athens, GR
- **Head of Division** of Computing Systems and Applications of the Department of Informatics and telecommunications, University of Athens, GR
- **Chairman and member** of several academic councils and delegates, GR, CY, EU
- **Director** of the Computer Centre Facilities of the University of Athens, GR

Teaching

Undergraduate: Introduction to Computer Science, Logic Design, Computer Architecture, Operating Systems, Expert Systems and Logic Programming, Artificial Intelligence, Theory of Computation, Games Theory, Complexity Theory, Introduction to Cryptography, Web programming, New Technologies and Museums.

Postgraduate: Advanced Computer Architecture, Expert Systems, Artificial Intelligence, Automated reasoning, Non-monotonic reasoning. Cryptography, Supercomputing, Object-Oriented Analysis - Design and Management, Research Methods

Supervision of theses: a large number of M.Sc. and Ph.D. theses.

R&D interests

A wide range of research interests. Research conducted in the following areas: Computer Architecture, HPCN, Logic design, VLSI design, Artificial Intelligence, Expert Systems, Knowledge Engineering, Logic Programming and Prolog machines, Data and Knowledge bases, Constraints-based programming, Combinatorial Optimization of Scheduling and Planning, Computer Networks, Multimedia and Hypermedia systems, Virtual Reality, Parallel computing, Parallel algorithms, Software Engineering, Systems Analysis and Design, e-Government, Document Management Systems, Affective Adaptive Educational Systems, Adaptive Visualization, Ontologies, Data Mining, Cryptography, Theory of Computation.

R&D Projects (funded ones)

Prof. Halatsis has participated, mostly as project leader, in several R&D projects funded by either the Commission of EU or Greek national funding bodies. The specific European projects are : SPAN of Esprit I (member of the UoA group), EDS of Esprit II (leader for the UoA group), PCA of Esprit II (member of the UoA group), SAFE of Delta (member of the UoA group), OSMOSE1 of Esprit I (co- leader of the UoA group), OSMOSE of Esprit II (co-leader of the UoA group), APPLAUSE of Esprit II (leader for the UoA group), GP-MIMD of Esprit II (co-leader of the UoA group), PARACHUTE of Esprit III (leader for the UoA group), MEMOIR of ESPRIT IV (co-leader of the UoA group), PARROT of ESPRIT IV (leader of the UoA group and co-technical coordinator of the whole project), SmartGov of IST (consortium leader). The Greek national programs which have been funded by the General

Secretariat of Research and Technology, the Ministry of Education and the Information Society belong to the categories of PENED, PRAXE and PYTHAGORAS (virtual reality and museums, handwritten character recognition, web logs mining, ontology visualization, document management and retrieval, adaptive user interfaces,). Also has been financed by the Olympic Airways for the development of Crew Scheduling of the flying personnel using Constraint Logic Programming CLP techniques. Recent R&D projects concern the development of Information systems for Historical Archives and Historical Museums in all the components of them, namely, classification, search, digitization and visualization with pioneering visualization and virtual reality methods.

Scientific activities

- Invited speaker in various national and international conferences.
- Invited lecturer in various tutorials/workshops.
- Chairman of the Steering Committee of the PARLE conferences and member of the Steering Committee of the EURO-PAR conferences.
- Member of Organizing Committees of various International Conferences.
- Referee in various scientific journals/conferences (IEEE, ACM, etc.)
- Consultant and advisor to various organizations (national/international).
- Participation in various CEC funded projects (among them project leader of the ESPRIT projects EDS, APPLAUSE, PARACHUTE, and PARROT, all HPCN projects), and GSRT funded projects.
- Evaluator/reviewer of various EU funded projects/programs.
- National Representative in the policy group of networks EUREKA/Cosine and Person in charge of the Greek Academic Network ARIADNI.
- Chairman of Committee of the Selection Committee for Academic Personnel for the Department of Information technology of University of Cyprus (up to 1994).
- Evaluator and Reviewer of projects of European Union, Greek GSRT, Ministry of Education.
- Main Designer of projects for Office Automation, e-Government Gateway, Data Warehouse and eID for the Cyprus Government (MoF).
- Main Designer of the Information System of Environment for the Greek Ministry of Environment, Planning and Public Works.
- Main designer of the building, laboratories, human and remaining infrastructure of the Departments of the Faculty of Sciences and Technology of the University of Peloponnese.
- Author of the Decennial Planning for the whole University of Peloponnese.
- Member of electoral bodies for academic positions for almost all the Greek Universities, as well as for awarding the doctoral diploma.
- Member of many Greek committees for drafting specifications, evaluation of offers for a lot of computing Systems of the Greek State and the Wider Public Sector.

Publications:

Author of an academic book for the Greek Open University on the Theory of Computation, co-author of two book chapters, author of lecture notes for all the lectures that have been delivered up today (included also the development relevant Internet sites for the recent lectures), translation of a widely used book in the Greek Universities, and author/co-author of more than 160 scientific papers after peer review in International Journals and Conference Proceedings. List is as follows:

PUBLICATIONS

Ph. D. Thesis

C. Halatsis, "Hardware Considerations of Executive and Information Retrieval Systems", Ph.D. Thesis, University of Manchester, Aug. 1971

Publication in scientific journals

1. G. Philokyprou and C. Halatsis, "Floating-Point and Multi-Bit Increment Digital Differential Analyser Structures", Electronics Letters, Oct. 1972, p. 531 – 532, <http://digital-library.theiet.org/content/journals/10>
2. C. Halatsis, G. Philokyprou and D. Maritsas, "Analysis of Block-Organized Buffers for Poisson Input and Periodic Block Output", Int. J. of Systems Science, vol 5, no 1, 1974, <http://dx.doi.org/10.1080/00207727408920074>
3. G. Philokyprou and C. Halatsis, "Electronic Buffer Memories", Int. J. of Electrical Engineering Education, vol 12, pp 25 - 36, 1975, <http://ije.sagepub.com/content/12/1/25.full.pdf+html>
4. C. Halatsis, G. Philokyprou and D. Maritsas, "Designing block-structured bubble-up buffers", Electronic Engineering, April 1976, pp 45-48.
5. G. Philokyprou, C. Halatsis and N. Gaitanis, "On the Problem of Finding d, t, r, and j Type Partition Pairs of a Sequential Machine", IEEE Transactions on Computers, March 1977.
6. C. Halatsis and G. Philokyprou, "Pseudo chaining in Hash Tables", Communications of the ACM 21(7), 554-557, July 1978.
7. C. Halatsis and A. Sokos, "Microprocessor-controlled Elevators", Electronic Engineering, Oct. 1978.
8. C. Halatsis and N. Gaitanis, "Irredundant Normal Forms and Minimal Dependence Sets of a Boolean Function", IEEE Transactions on Computers, Nov. 1978.
9. C. Halatsis and N. Gaitanis, "On the minimization of the Control Store in Microprogrammed Computers", IEEE Transactions on Computers, Dec. 1978.
10. C. Halatsis, M. Sigala and G. Philokyprou, "Polylinear Decomposition of Synchronous Sequential Machines", IEEE Transactions on Computers, Dec. 1978.
11. N. Gaitanis and C. Halatsis, "A new Double-Rank Realization of Sequential Machines", IEEE Transactions on Computers, Dec. 1978.
12. C. Halatsis, M. Sigala and C. Cambakis, "A simple computer-assisted text composition system", Angewandte Informatik, Dec. 1978.
13. C. Halatsis and N. Gaitanis, "Positive Fail - Safe Realization of Synchronous Sequential Machines", IEEE Transactions on Computers, Febr. 1979.
14. N. Gaitanis, C. Halatsis, M. Sigala, "Fail Safe Counters", Journal of Digital Processes, no 5, 1979.
15. A.C. Arvillias, D.G. Maritsas and C. Halatsis, "Microcomputer Implemented Random and Key Stream Generating Mechanisms", Euromicro Journal, 1980.
16. N. Gaitanis and C. Halatsis, "Negative Fail-Safe Sequential Circuits", Electronics Letters, vol 16, no 16, July 1980.
17. A. vanDam, M. Barbacci, C. Halatsis, J. Joosten and M. Letheren, "Simulation of a Horizontal Bit-Slice Processor using the ISPS Architecture Simulation Facility", IEEE Transactions on Computers, July 1981.
18. C. Halatsis, N. Gaitanis and M. Sigala, "Error-Correcting Codes in Binary-Coded Radix-r Arithmetic", IEEE Transactions on Computers, March 1983.
19. N. Gaitanis and C. Halatsis, "A New Design Method for m-out-of-n Totally Self-Checking Checkers", IEEE Transactions on Computers, March 1983.

20. N. Gaitanis and C. Halatsis, "Near-Perfect Codes for Binary Coded Radix-r Arithmetic Units", IEEE Transactions on Computers, May 1983.
21. C. Halatsis, N. Gaitanis and M. Sigala, "Fast and Efficient TSC-Checkers for m-out-of- $(2m \pm 1)$ codes", IEEE Transactions on Computers, May 1983.
22. A. Hatzopoulos and C. Halatsis, "Microprocessor-based FIR Spectrophotometer", Review of Scientific Instruments, 55(9), Sept. 1984.
23. C. Efstathiou and C. Halatsis, "Efficient Modular Design of m-out-of-2m TSC Checkers, for $m=2^k-1, k>2$ ", Electronics Letters, vol 21, no 23, 1985.
24. A. Pombortsis and C. Halatsis, "Performance Analysis of Interconnection Networks of a Modified Model for Synchronous Multiprocessors", Electronics Letters, vol 22, no 4, 1986.
25. A. Pombortsis and C. Halatsis, "Analysis of a Modified Model for Synchronous Multiprocessor Systems", The Journal of Systems and Software, no 6, pp 361-365, 1986.
26. A.M. Paschalis, C. Halatsis and G. Philokyprou, "Concurrently Totally Self-Checking Microprogram Control with Duplication of the Microprogram Sequencer", Euromicro Journal, Microprocessing and Microprogramming, no 20, pp 271-281, 1987.
27. J. Vlachavas and C. Halatsis, "L-Machine: a low cost personal sequential inference machine", The Journal of Systems and Software, 1988.
28. A.M. Paschalis, D. Nikolos and C. Halatsis, "Efficient Modular Design of TSC Checkers for m-out-of-2m codes", IEEE Transactions on Computers, March 1988.
29. A. Pombortsis and C. Halatsis, "Performance of crossbar interconnection networks in the presence of hot spots", IEE Electronics Letters, vol 24, No 3, Febr. 1989.
30. A. Pombortsis and C. Halatsis, "Behavior of circuit-switched Multistage Networks in presence of memory hot spots", IEE Electronics Letters, vol 25, No 13, June 1989.
31. A.M. Paschalis, C. Efstathiou and C. Halatsis, "An Efficient TSC 1/3 Code Checker", IEEE Transactions on Computers, March 1990.
32. P. Stamatopoulos, I. Karali, C. Halatsis, "A Tour Advisory System Using a Logic Programming Approach", Applied Computing Review (ACR), Special Issue on Logic Programming Applications, Sept. 1993.
33. A. Pombortsis and C. Halatsis, "Performance of Circuit-Switched Interconnection Networks Under Non uniform Traffic Patterns", The Journal of Systems and Software, Vol. 20, No 2, Feb. 1993.
34. A. Tsalgatidou, D. Gouskos, C. Halatsis, "Towards the Development of Effective and Flexible Information Systems", Journal of Information Systems, Vol. 1, No 2, 1995.
35. A. Tsalgatidou, C. Halatsis, M. Spiliopouloy, M. Hatzopoulos, "A Multimedia Title Development Environment (MTDE)", Int. Journal of Information Processing & Management, Vol 31, No 1, 1995 (Pergamon Press).
36. Y. Tsiarouhas, A. Paschalids, D. Nikolos, and C. Halatsis, "Robust Test Generation for Transistor Stuck-Open Faults in CMOS Complex Gates", Int. J. of Electronics, Vol. 79, No 2, pp 129-142, 1995.
37. E. Karkaletsis, C. Spyropoulos, G. Vouros, C. Halatsis, "Organization and Exploitation of Terminological Knowledge in Software Localization", TermNet News (TNN), the Journal of International Cooperation in Terminology, No 48, March 1995.

38. Y. Tsiatouhas, T. Haniotakis, C. Halatsis, A. Arapoyianni, "Design of stuck-open fault testable CMOS complex gates", *Electronics Letters*, Vol. 32, No 4, pp 315-317, 1996.
39. D. Gizopoulos, D. Nikolos, A. Paschalis, C. Halatsis, "C-Testable Modified Booth Multipliers", *J of Electronic Testing: Theory & Applications (JETTA)* Vol. 8, No 3, pp 241-260, June 1996.
40. D. Gizopoulos, A. Paschalis, D. Nikolos, C. Halatsis, "Linear-Testable and C-testable $N_x \times N_y$ Modified Booth Multipliers", *IEE Proc. - Computers & Digital Technique*, Vol. 143, No 1, pp 44-48, Jan 1996.
41. I. Voyiatzis, A. Paschalis, D. Nikolos, C. Halatsis, "An Efficient Built-in Self Test Method for Robust Path Delay Testing", *J of Electronic Testing-Theory & Applications* pp 219-222, June 1996.
42. Y. Tsiatouhas, Th. Haniotakis, D. Nikolos, A. Paschalis and C. Halatsis, "Hierarchical Robust Test Generation for CMOS Circuit Stuck-Open Faults", *International J. of Electronics*, Vol. 82, No 1, pp 45-60, 1997.
43. Th. Haniotakis, A. Paschalis, C. Halatsis, G. Philokyprou, "Testable designs of One-Count Generators", *International J. of Electronics*, vol. 85, No. 5 , pp. 629-650, 1998.
44. D. Gizopoulos, A Paschalis, D. Nikolos, and C. Halatsis, "On robust Two-pattern testing of One-dimensional CMOS Iterative Logic Arrays", *Int. Journal of Electronics*, vol. 86, no 8, pp 967-978, August 1999.
45. I. Vlahavas, P. Kefalas, C. Halatsis, "OASys: An AND/OR parallel logic programming system", *Parallel Computing* 25, pp.321-336, 1999.
46. I. Voyiatzis, A Paschalis, D. Nikolos, and C. Halatsis, "Accumulator-Based BIST Approach for Two-Pattern Testing", *Journal of Electronic Testing, Theory and Applications*, vol. 15, no 3, pp 267- 278, December 1999.
47. I. Voyiatzis, N. Kratinis, D. Gizopoulos, A Paschalis and C. Halatsis, "Accumulator-based Built-In Self-Test Generator for Robustly Detectable Sequential Fault Testing", *IEE Proceedings Computers & Digital Techniques*, Nov. 2004.
48. I. Voyiatzis, A Paschalis, D. Gizopoulos, N. Kratinis and C. Halatsis, "A Concurrent Built-In Self-Test Architecture Based on a Self-Testing RAM", *IEEE Transactions on Reliability*, March 2005.
49. I. Voyiatzis and C. Halatsis, "A low-cost Concurrent BIST scheme for increased Dependability", *IEEE Transactions on Dependable and Secure Computing*, April-June 2005.
50. C. Vassilakis, G. Lepouras, C. Halatsis and T. P. Lobo, "An XML model for electronic services", *Electronic Government*, Vol. 2, No.1 pp. 41 – 55, 2005
51. George Lepouras, Costas Vassilakis, Constantin Halatsis and Panagiotis Georgiadis, "Domain Expert User Development: The SmartGov Approach", *Comm. of ACM*, 2005
52. I. Voyiatzis, Th. Haniotakis, C. Halatsis, "Algorithm for the Generation of SIC Pairs and its Implementation in a BIST environment", *IEE Proc. Circuits, Devices & Systems*, vol. 153, Issue 5, October 2006, pp. 427-432.
53. Stergos D. Afantenos, Vangelis Karkaletsis, Panagiotis Stamatopoulos and Constantin Halatsis, "Using synchronic and diachronic relations for summarizing multiple documents describing evolving events", *Journal of Intelligent Information Systems*, March 14, 2007

54. C. Vassilakis, G. Lepouras and C. Halatsis, "A knowledge-based approach for developing multi-channel e-government services", *Electronic Commerce Research and Applications* 6 (2007) 113–124
55. V. Katifori, C. Halatsis, G. Lepouras, C. Vassilakis, E. Giannopoulou, "Ontology Visualization Methods – A survey", *ACM Computing Surveys*, October 2007
56. I. Voyiatzis, A. Paschalis, D. Gizopoulos, C. Halatsis, E. Makri, M. Hatzimihail, "An Input Vector Monitoring Concurrent BIST Architecture Based on a Pre-computed Test Set", *IEEE Transactions on Computers*, Volume 57, Issue 8, Aug. 2008, pp.1012 - 1022.
57. G. Louloudis, B. Gatos, I. Pratikakis & C. Halatsis, "Text line detection in handwritten documents", *Pattern Recognition Journal*, Volume 41, Issue 12 (December 2008), pp. 3758-3772.
58. G. Louloudis, B. Gatos, I. Pratikakis & C. Halatsis, "Text line and word segmentation of handwritten documents", *Pattern Recognition*, vol. 42 (issue 12), pp.3169-3183, 2009
59. Petrilis D, Halatsis C. (2008), "Two-level clustering of web sites using self-organizing maps", *Neural Process Lett* 27(1):85-95
60. Elena Torou, Akrivi Katifori, Costas Vassilakis, George Lepouras, Constantin Halatsis, *Historical research in archives: user methodology and supporting tools*, *Int. J. on Digital Libraries* Vol. 11 No. 1 Pg. 25-36, 2010.
61. Leontidis, M., Halatsis, C., Grigoriadou, M. (2011). "Using an Affective Multimedia Learning Framework for Distance Learning to Motivate the Learner Effectively", *International Journal of Learning Technology*, Vol 6(3), 223-250.
62. Masvoula M., Halatsis C., and Martakos D. (2011): Predictive automated negotiators employing risk-seeking and risk-averse strategies, *IFIP Advances in Information and Communication Technology*, Volume 363/2011, 325-334.

Publication in Conference proceedings

1. D. Maritsas, G. Philokyrou and C. Halatsis, "On-line Scanning- System Design Considerations", *Proceedings Int. Symposium INFORMATICA 75*, Bled, Yugoslavia, Oct. 1975.
2. G. Philokyrou, C. Halatsis, M. Sigala and N. Gaitanis, "Synthesis and Applications of Boolean Memories", *Proceedings Int. Symposium INFORMATICA 75*, Bled, Yugoslavia, Oct. 1975.
3. G. Philokyrou, N. Gaitanis and C. Halatsis, "Generalized Setting Equations for the Memory Elements of Sequential Machines -Self-Independence Criteria", *Proceedings Int. Symposium INFORMATICA 76*, Bled, Yugoslavia, Oct. 1976.
4. C. Halatsis and M. Sigala, "Counting Properties of the Switch-Tail Shift-registers", *Proceedings Int. Symposium INFORMATICA 78*, Bled, Yugoslavia, Oct. 1978.
5. N. Gaitanis, C. Halatsis and G. Philokyrou, "Optimal Conversion of a Separating System of a Finite Set to a Completely Separating System", *Proceedings Int. Symposium INFORMATICA 78*, Bled, Yugoslavia, Oct. 1978
6. C. Halatsis, A. vanDam, J. Joosten and M. Letheren, "Architectural Considerations for a Microprogrammable Emulating Engine using Bit - Slices", *Proceedings 7th Int. Symposium of Computer Architecture*, La Baule, France, May 1980, also as CERN report DD/79/7.
7. by J. Anthonioz-Blanc, C. Halatsis, J. Joosten, M.F. Letheren, A. vanDam, A. vanPraag and C. Verkerk, "MICE, a Fast User Microprogrammable Emulator of

- the PDP-11”, presented at the Posters session of the Int. Conf. on Experimentation for LEP, Uppsala, June 1980.
8. C. Halatsis, invited paper, “Three-level Totally Self-Checking Checkers for m-out-of-(2m± 1) codes”, Proceedings IEEE Int. Conf. on Circuits and Systems, ICCS 80, New York, Oct. 1980.
 9. A. vanDam, M. Barbacci, C. Halatsis, J. Joosten and M. Letheren, “Simulation of a Horizontal Bit-Slice Processor: The MICE Experience” IFIP TC - 10 Proceedings 5th Int. Conf. On CHDL’s and their applications, Kaiserlantern, North - Holland, Sept. 1981.
 10. N. Gaitanis and C. Halatsis,
 11. “Negative realization of Fail-Safe Counters”, Proceedings Int. Symposium INFORMATICA 81, Bled, Yugoslavia, Oct. 1981
 12. C. Halatsis, invited paper, “Highly Concurrent Computing Structures”, by Proceedings, Conf. on Specialized Processors, Padova, April 1983.
 13. C. Efstathiou and C. Halatsis, “Modular Realization of m-out-n TSC Checkers”, Proceedings 13th Int. Symposium on Fault Tolerant Computing, FTCS 13, Milano, June 1983.
 14. C. Efstathiou and C. Halatsis, “Modular Design of Totally Self-Checking Checkers for 1-out-of-n codes”, Proceedings Second GI/NTG/GMF Conf. on Fault Tolerant Computing Systems, Bonn, Sept. 1984.
 15. M. Gavalas, A. Arvillias and C. Halatsis, “Hardware implementation of a unification algorithm for a PROLOG system”, Proceedings IX Symposium in Informatics, Jahorina, Yugoslavia April 1985.
 16. A.M. Paschalis, N. Nikolos and C. Halatsis, “Efficient Modular Design of TSC Checkers for m-out-of-2m codes”, Proceedings Aegean Workshop on Computing, VLSI Algorithms and Architectures, AWOG 86, Loutraki, July 1986, also in LNCS Vol 227, Springer Verlag, 1986.
 17. A. Pombortsis, P. Linardis and C. Halatsis, “Study of a Class of Conflict Resolution Strategies for Synchronous Multiprocessor Interconnection Networks”, Proceedings 12th Symposium on Microprocessing and Micropogramming, EUROMICRO 86, Venice, Sept. 1986.
 18. A. Pombortsis, P. Linardis and C. Halatsis, “On the Performance of Partitionable Multistage Interconnection Networks for Multiprocessor Systems”, Proceedings Integrated Circuit Technology Conference, Limerick, Irland, Sept. 1986.
 19. A.M. Paschalis, C. Halatsis and G. Philokyprou, “Towards concurrently Totally Self-Checking Microprogram Control Units”, Proceedings of the 1st European Workshop on Fault Diagnostics, Reliability and Related Knowledge – Based Approaches, Rhodes, Sept. 1986, Also in Fault Diagnostics, Reliability and Related Knowledge – Based Approaches, Vol2, D.Reidel Publishing Company, pp357-368, 1987
 20. J. Vlachavas and C. Halatsis, “A New Abstract Prolog Instruction Set”, Proceedings Avignon 87, Expert systems and their applications, Avignon, May 13-15, 1987.
 21. I. Stamelos and C. Halatsis, “Efficient Test Generation for Register Transfer Level Descriptions”, Proceedings Third Int. GI/NTG/GMR Conference on Fault-Tolerant Computing Systems, Bremerhaven, Sept. 9-11, 1987.
 22. A. Pombortsis, P. Linardis and C. Halatsis, “Study of A Resource Arbitration - Interconnection Network for Multiprocessor Systems”, Proceedings 1987 CompEuro Conference, VLSI and Computers, COMP EURO 87, Hamburg May 1987.

23. D. Stamatis and C. Halatsis, "Encapsulation Constructs in Prolog", Proceedings Euromicro 87, 13th symposium on Microprocessing and Microprogramming, Portsmouth, Sept. 14-17, 1987.
24. J. Vlachavas and C. Halatsis, "A RISC Prolog Machine Architecture", Proceedings Euromicro 87, 13th symposium on Microprocessing and Microprogramming, Portsmouth, Sept. 14-17, 1987.
25. A. Pombortsis, J. Vlachavas and C. Halatsis, "On the Performance of Packet Switching Interconnection Networks for Multiprocessor Systems", Proceedings Int. Conf. on Parallel Processing and Applications, L' Aquila, Italy, Setp. 23-25 1987.
26. A. M. Paschalis, C. Halatsis and G. Philokyrou, "Towards Concurrently Totally Self-Checking Microprogram Control Units", System Fault Diagnostics, Reliability and Related Knowledge-Based Approaches, Vol. 2, D. (edited by S. Tzafestas, M. Singh and G. Schmidt),Reidel Publishing Company, 1987, pp.357-368
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Acknowledgements

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Lecture books/notes

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