INSTITUTION	NATIONAL AND KAPODISTRIAN UNIVERSITY OF ATHENS					
SCHOOL	SCHOOL OF SCIENCE					
DEPARTMENT	INFORMATICS AND TELECOMMUNICATIONS					
COURSE LEVEL	UNDERGRADUATE					
COURSE TITLE	**Logic Design Lab**					
COURSE CODE	**K02ε**		**Semester**	1	**ECTS**	2
TEACHING HOURS per week	**THEORY**		**SEMINAR.**		**LABORATORY**	2hours/group
COURSE TYPE	**Select one of the following and delete the rest** Optional Lab (EP) **K** | **E1** | **E2** | **E3** | **E4** | **E5** | **E6** A-B | | | | | | | *Fill the table as in the curriculum:* Track (A-Computer Science, B- Computer Engineering) / Specialization Compulsory (Y) / Core Specialization (B)/ Elective Specialization (E)					
URL	https://eclass.uoa.gr/courses/DI375					
EXPECTED PRIOR KNOWLEDGE/ PREREQUISITES AND PREPARATION:						
TEACHING AND EXAMINATIONS LANGUAGE:	GREEK					
THE COURSE IS OFFERED TO ERASMUS STUDENTS	NO					

COURSE CONTENT
This course is about digital circuits design and implementation using Field Programmable Gate Arrays (FPGAs) technologies using CAD tools from Xilinx (Vivado Design Suite WebPACK edition). In details, the course is about digital circuits design using the VHDL hardware description language, under specific timing and I/O constraints, synthesis, implementation and bitstream generation targeting specific FPGA target technology, as well as, verification at all levels of development (VHDL source code, post synthesis, post place & route) using simulation, debug and FPGA validation using a proper FPGA development board. The digital circuits to be designed and implemented are of similar academic importance and complexity to those taught in the undergraduate course of Logic Design (K02). The development board that will be used in the training process is the Xilinx Zedboard hosting a Xilinx Zynq 7000 series FPGA. The course includes the following sections:

1. Digital system implementation technologies - Introduction to Xilinx FPGA technology
2. Methodology and FPGA development flow
3. Downloading, licensing and installation of Xilinx FPGA development tools. Introduction to development board (Zedboard)
4. Basic concepts of modeling with VHDL
5. Basic verification using VHDL testbenches
6. Basic combinational circuits (decoders, encoders, multiplexers, etc.) with VHDL
7. Basic arithmetic operations (addition, subtractions, comparisons, multiplications, etc.) with VHDL
8. Basic state elements (latches, flip-flops, registers, shift registers) with VHDL
9. Counters with VHDL
10. Memories with VHDL
11. Finite State Machines with VHDL
12. Timing constraints and design for timing closure
13. Design using Xilinx IP cores

STUDENT LEARNING OBJECTIVES
Teaching-Learning Goals-Expected Learning Outcomes Upon successful completion of the course the student will be able to: • Design and implement digital circuits using VHDL hardware description language • Design and implement digital circuits targeting FPGA technologies using Xilinx software tools • Understand the synthesis, verification and implementation processes targeting FPGAs

TEACHING AND LEARNING METHODS - ASSESSMENT	
TEACHING METHOD	In the classroom using PowerPoint slide presentations for the theoretical part of the course (VHDL hardware description language). In the laboratory for the design and implementation of circuits on the FPGA development board.
USE OF INFORMATION AND COMMUNICATION TECHNOLOGIES	Learning process supported by the e-class platform (Hardware delivery, Announcements) Email communication Utilization of Specialized Software
TEACHING ORGANIZATION *Describe in detail the way and methods of teaching:* *Enhanced Lectures,* *Online Lectures,* *Seminars,* *Tutorial,* *Laboratory,* *Laboratory Exercise,* *Study & analysis of literature,* *Practice (Positioning),* *Interactive teaching,* *Developing a project,* *Individual / group work* *Telework (reference to tools) etc.*	

Activity	***Student Workload*** *(hours)*
Lectures	12
Laboratory	14
Independent Study	26
Total Course	***52***

Details of the student's study hours for each learning activity and hours of non-guided study are shown to ensure that the total workload at the semester corresponds to the ECTS	
ASSESSMENT OF STUDENTS *Description of the assessment process* *Assessment Methods, Formative or Concluding, Multiple Choice Test, Quick Response Questions, Test Development Questions, Problem Solving, Written Work, Report / Report, Oral Examination, Public Presentation, Laboratory Work, Other / Other* *Fully defined evaluation criteria are mentioned and if and where they are accessible to students.*	Describe explicitly methods, evaluation tools and provided feedback. The table below is supplemented accordingly.

Assessment methods	***Number***	***Percentage***
Laboratory examination	1	100%

LITERATURE AND STUDY MATERIALS / READING LIST
1) Digital Design (VHDL): An Embedded Systems Approach Using VHDL, Peter J. Ashenden, (In Greek by M.Psarakis, N. Kranitis and D. Gizopoulos), 1st Edition, 2010, New Technologies Publications 2) Circuit Design with VHDL, V.A. Pedroni, 1st Edition, 2008, Kleidarithmos Publications