

## **COURSE SYLLABUS**



INSTITUTION	NATIONAL AND KAPODISTRIAN UNIVERSITY OF ATHENS								
SCHOOL	SCHOOL OF SCIENCE								
DEPARTMENT	INFORMATICS AND TELECOMMUNICATIONS								
COURSE LEVEL	UNDERGF	UNDERGRADUATE							
COURSE TITLE	Compute	Computer Architecture II							
COURSE CODE	К30		Semes	Semester 5		ECTS	e	5	
TEACHING HOURS per week	THEORY	3	SEMIN	AR.	1	LABORATO	DRY	1	
	Select one of the following and delete the rest Compulsory (YM)								
COURSE TYPE	K	E1	E2	E3		E5	E	6	
	B   B   Y  Fill the table as in the curriculum: Track (A-Computer Science, B- Computer Science) / Specialization Compulsory (Y) / Core Specialization (Elective Specialization (E)							B- Computer	
		• .		n Con	-	(Y) / Core Sp	ecia	-	
URL		pecializat	ion (E)		npulsory	(Y) / Core Sp	ecia	-	
URL  EXPECTED PRIOR  KNOWLEDGE/ PREREQUISITES  AND PREPARATION:	Elective S	pecializat	ion (E) gr/cours	es/D5	npulsory	(Y) / Core Sp	ecia	-	
EXPECTED PRIOR KNOWLEDGE/ PREREQUISITES	Elective S https://ed	pecializat	ion (E) gr/cours	es/D5	npulsory	(Y) / Core Sp	ecia	-	

## **COURSE CONTENT**

ISA of RISC architectures (review)

Basics of pipelining,

Pipelining in MIPS microprocessors.

Datapath and control unit design for pipelined CPU.

Data, control and structural hazards.

Superscalar and out-of-order basics.

Branch prediction.

### **COURSE SYLLABUS**





Cache memories concept.

Caches architectures and algorithms.

Virtual memory.

Input/output devices.

Storage devices performance and reliability.

Microprocessor systems interfacing.

#### STUDENT LEARNING OBJECTIVES

Teaching-Learning Goals-Expected Learning Outcomes

Introduction to advanced computer architecture topics including pipelining, caches and input/output and storage devices.

Upon successful completion of the course the student will be able to:

- Mention advanced techniques for performance improvement
- Describe the concept and implementation details of pipelining
- Use architectural simulators for pipelining
- Explain the basics and the implementation of caches
- Implement hardware and software techniques for caches performance improvement
- Use architectural simulators for caches

TEACHING AND LEARNING METHODS - ASSESSMENT						
TEACHING METHOD	In Class with slides and whiteboard for examples and exercises of the course.  In the PCs Lab using educational architectural simulators.					
USE OF INFORMATION AND COMMUNICATION TECHNOLOGIES	Electronic platform e-class (all tools employed: announcements, documents, assignments, groups of users, etc.) Email communication Live broadcasting of lectures Recording of lectures for offline study					
TEACHING ORGANIZATION  Describe in detail the way and methods of teaching:  Enhanced Lectures.	Activity	Student Workload (hours)				
Online Lectures,	Lectures	39				
Seminars,	Tutorial	13				
Tutorial, Laboratory,	Laboratory 13					
Laboratory, Laboratory Exercise, Study & analysis of literature,	Lab preparation 11					
Practice (Positioning),	Graded assignments 35					
Interactive teaching, Developing a project,	Independent Study 39					



# **COURSE SYLLABUS**



40% (20% each)

Individual / group work Telework (reference to tools) etc.  Details of the student's study hours for each learning activity and hours of non-guided study are shown to ensure that the total workload at the semester corresponds to the ECTS	Total Course (25 hours of workload pe of credit)	er unit	150		
ASSESSMENT OF STUDENTS Description of the assessment process	Describe explicitly methods, evaluation tools and provided feedback. The table below is supplemented accordingly.				
Assessment Methods, Formative or Concluding, Multiple	Assessment methods	Number	Percentage		
Choice Test, Quick Response Questions, Test Development	Written examination	1	60%		
Questions, Problem Solving, Written Work, Report / Report, Oral Examination, Public Presentation, Laboratory Work, Other / Other					

Assignments (on

simulators)

## LITERATURE AND STUDY MATERIALS / READING LIST

Fully defined evaluation criteria are mentioned and if and

where they are accessible to students.

"Computer Organization and Design: the Hardware/Software Interface", 4<sup>th</sup> Edition, D.A.Patterson, J.L.Hennessy, Elsevier/Morgan Kaufmann, 2010.